IN THE SPECIFICATION

Please replace the paragraph beginning on page 1, lines 15 to 23, with the following:

As semiconductor devices have been developed to have a high degree of integration, patterns formed on the chip have become smaller in size, resulting in the space between the patterns becoming narrower. In the past, polysilicon was a very useful material as a wiring material such as in a gate electrode or a bit line. However, as the patterns become gradually smaller, the resistivity in the polysilicon increases, resulting in larger RC time delays and IR voltage drops. In order to improve ~~the~~ a short channel effect and punch through caused by a decrease in the gate length of a transistor, junction depths of source/drain regions should be shallower while parasitic resistances of source/drain regions, such as sheet resistances and contact resistances, should be reduced.

Please replace the paragraph beginning on page 1, lines 30 to 34, with the following:

For non-volatile memory devices having a ~~vertically~~ vertical gate stack structure including a tunnel dielectric layer, a floating gate, a dielectric layer and a control gate stacked successively on a silicon substrate, as the design rule decreases to about 0.1μm less, the silicide layer such as cobalt silicide ($CoSi_2$) is selectively formed only on the gate electrode by the silicide process so as to reduce the resistance of the control gate serving as a word line.

Please replace the paragraph beginning on page 2, lines 9 to 12, with the following:

However, as the spaces between the gates in the memory cell becomes narrower, with a reduction in the design rule to about 0.12μm or less, the coupling ratio lowers due to a parasitic capacitance generated between the gates. This results in an oxide spacer having a dielectric constant lower than that of silicon nitride to be used as the gate spacer.

Please replace the paragraph beginning on page 3, lines 1 to 3, with the following:

Then, an oxide layer 20, e.g. a high temperature oxide (HTO) layer, is deposited to a thickness of about 1200~1500Å on the gate stack structures 30 and the substrate 10 by a chemical vapor deposition (CVD) process.

Please replace the paragraph beginning on page 3, lines 33 to 34, with the following:

The present invention provides a method of preventing the void generation between gates manufacturing a non-volatile memory device.